REMARKS

In th present application, claims 1-36 are pending. Claims 10, 20, 21, 22, 23 and 26 have been amended. Claims 13, 14, 17, 18 and 19 ar canceled herein. New claims 69-77 are added herein.

35 U.S.C. §112

Claims 23 and 34-36 were rejected under 35 U.S.C. §112, second paragraph for being indefinite.

Claim 23 has been amended herein to recite that the floating gate is formed over the p-type layer such that at least a portion of the floating gate overlies at least a portion of the second n-type layer. As claimed, the second n-type layer is formed in the p-type layer. The applicant believes that claim 23 is definite as amended herein and thus requests that the Examiner withdraw the rejection of claim 23 under 35 U.S.C. §112, second paragraph.

Claim 34 depends from claim 26. Claim 26 has been amended herein to reflect that a second n-type layer is formed in a p—type layer defining a drain. As such, proper antecedent basis is provided to recite "the drain" in the first line of claim 34. Accordingly, the applicant requests that the Examiner withdraw the rejection of claim 34 under 35 U.S.C. §112, second paragraph.

Claims 35 and 36 each depend from claim 26. Claim 26 has been amended herein to recite a floating gate formed over the p-type layer so as to avoid the select trench. As such, proper antecedent basis is provided to recite "the floating gate" in the first line of claim 35 and in the first line of claim 36. Accordingly, the applicant requests that the Examiner withdraw the rejection of claims 35 and 36 under 35 U.S.C. §112, second paragraph.

35 U.S.C. §102

Claims 10-14, 17-19, 22 and 26-28 wer rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,998,261 (hereinafter "Hofmann"). According to the M.P.E.P. §706.02, in order to be anticipating under §102, the reference must teach every aspect of the claimed invention. *Carella v. Starlight Archery and Pro Line Co.*, 804 F.2d 135, 138, 231 U.S.P.Q. 644, 646 (Fed. Cir. 1986).

Hofmann teaches a vertically stacked MOS structure wherein the floating gate is formed in the same trench as the select gate (See floating gates 11 and select gate 13 formed in trench 7 in Figs. 5; Col. 2, lines 19-29; Col. 5, lines 7-9 and 15-17; Abstract).

Discussion of Claim 10:

However, Hofmann fails to anticipate claim 10 as amended herein. For example, claim 10 has been amended to recite that the source and drain are arranged substantially vertically and the gate is horizontally positioned such that at least a portion of the gate overlies at least a portion of the drain. As pointed out above, and as best seen in Fig. 5, the floating gates 11 are formed in trench 7 and are thus not horizontally positioned at all. Particularly, each trench is lined with a first dielectric layer 10 (Col. 4, lines 24-26). Doped polysilicon spacers 11 (floating gates) are formed in the flanks of the trench 7 (Col. 4, lines31-34). A second dielectric layer 12 is then conformally deposited over the substrate (Col. 4, lines 51-55; Fig. 5).

Claim 10 has been further amended to recite that the gate of the select transistor is formed substantially vertically and perpendicular to the gate of the first transistor relative to a vertical plane. In the Office Action on page 3, paragraph 8, the Examiner asserts that the select transistor gate 13a is substantially perpendicular to the first transistor gate 11. The applicant respectfully traverses this interpretation of Hofmann. In Hofmann, reference 13 is a polysilicon layer that includes two functions, that of acting as the control gates, and that of acting as word lines. The word lines are designated 13a, apparently to distinguish this function. After a doped layer of polysilicon 13 is deposited over the substrate, a word line mask is aligned over the polysilicon 13, and

the structure is etched to define word lines 13a extending *transversely* to the trenches (best s en in the plan view of Fig. 6). The polysilicon in the tr nches 7 defines the control gat s. As such, the word lines 13a are transversely displaced from the floating gates 11, but the control gate 13, which is formed *in the trench* 7, is parallel to the floating gates 11 (Col. 5, lines 7-8).

Accordingly, the applicant requests that the Examiner withdraw the rejection of claim 10 and the claims that depend therefrom, including claims 11-12, under 35 U.S.C. §102(b).

Discussion of Claims 13, 14, 17, 18 and 19:

Claims 13, 14, 17, 18 and 19 have been canceled herein. Accordingly the rejections thereto are moot.

Discussion of Claim 22:

Hofmann fails to anticipate claim 22 as amended herein. For example, claim 22 has been amended to recite that a floating gate is formed over a tunnel oxide layer such that at least a portion of the floating gate overlies at least a portion of the drain. As pointed out above, Hofmann teaches the formation of the floating gates and the control gate in the trench. As such, the floating gates taught by Hofmann are not formed over a tunnel oxide. Moreover, the floating gates taught by Hofmann do not overlie at least a portion of the drain.

Further, Hofmann does not teach a select gate formed along sidewalls of the select trench. Rather, as can be seen in Fig. 5 of Hofmann, a trench 7 includes a pair of floating gates 11 formed on opposite sidewalls. A control gate 13 is formed parallel to the floating gates 11 within the trench 7 such that a dielectric layer 12 insulates the control gate 13 and the floating gates 11 from one another. The control gate 13 in the trench 7 is thus spaced from the sidewalls of the trench by insulating layer 12, floating gates 11, and the insulating layer 10.

Still further, claim 22 has been amended to remov the limitation that the floating gate be "self-aligned. Moreover, this amendment renders moot the Examiner's interpretation of the r citation as a product by process claim.

Also, claim 22 is further amended herein to clarify that the select gate is formed in a select trench, and the active trench is formed generally over the drain and a conductive material is formed in the active trench. Accordingly, the applicant requests that the Examiner withdraw the rejection of claim 22 under 35 U.S.C. §102(b).

Discussion with Respect to Claim 23:

Hofmann fails to anticipate claim 23 as amended herein. While the Examiner did not provide any comments with respect to claim 23, the applicant points out for example, that Hofmann does not teach a floating gate formed over the p-type layer such that at least a portion of the floating gate overlies at least a portion of the second n-type layer. As discussed in greater detail above, Hofmann teaches vertical floating gates formed in trenches.

Hofmann further fails to teach wordlines formed over the substrate and the digitlines. As is best seen in Fig. 5, the word lines 13 are formed over the substrate, but are not formed over the bitlines. In fact, the bitlines are not discussed or illustrated at all in Hofmann. Accordingly, the applicant requests that the Examiner withdraw the rejection of claim 23 under 35 U.S.C. §102(b).

Discussion with Respect to Claim 26:

Hoffman fails to anticipate claim 26 as amended herein. For example, claim 26 has been amended herein to recite a floating gate formed over the p-type layer so as to avoid the select trench. As discussed more thoroughly above, Hofmann teaches the floating gates formed in a trench within the p-type layer. The floating gates are not formed over the p-type layer. Accordingly, the applicant requests that the Examiner withdraw the rejection of claim 26 and the claims that depend therefrom, including claims 27 and 28, under 35 U.S.C. §102(b).

DOUBLE PATENTING

With respect to the double patenting objection, the applicant has canceled both claims 17 and 18 herein. As such, the double patenting objection is moot.

ALLOWABLE SUBJECT MATTER

The applicant would like to thank the Examiner for the early indication of allowable subject matter in claims 1-9, 15, 16, 20, 21, 24, 25 and 29-33. As a clarification to the Examiner's statement of reasons for the indication of allowable subject matter, the applicant points out that claim 1 recites that the floating gate need only overly at least a portion of the drain. Similarly, claim 21 defines the horizontal floating gate in terms of the tunnel oxide and first poly layers. The tunnel oxide is formed over at least a portion of the second n-type layer.

Claims 15, 16 and 20, 24 and 25 recite that the horizontal floating gate is formed over the substrate, but need not necessarily align over the drain.

Claims 20 and 21 are amended herein to correct a minor issue. As amended, the trench for the select gate is formed in the p-type layer. Also, claim 21 has been amended to reflect that the tunnel oxide is formed over the second n-type layer. Exemplary but non-limiting support for this correction is found in Figs. 2A and 8A.

Claims 29-33 depend from claim 26. Claim 26 as amended herein recites that the floating gate is formed over the p-type layer so as to avoid the trench. However, claim 26 is not limited to positioning the horizontal floating gate over the drain.

New Claims:

New claim 69 is patentable over the art of record, and in particular, Hofmann. For example, non of the art of record teaches or suggests a first floating gate formed over a first layer adjacent to a trench and proximate to a first substantially vertical

channel. New claims 70-73 depend from claim 69. New claim 74 is also patentable over the art of record. For example, claim 74 recites a floating gat formed over a second layer adjacent to a trench. Claims 75-77 depend from claim 74.

CONCLUSION

The applicant respectfully submits that the pending claims represent allowable subject matter. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
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Appendix A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

10. (Amended) A memory cell having a square feature size of less than $4.5F^2$ comprising:

a first transistor comprising a source, a drain and a gate, wherein the source and drain are arranged substantially vertically and the gate is horizontally positioned such that at least a portion of the gate overlies at least a portion of the drain; and

a select transistor coupled to the first transistor, comprising a source, a drain and a gate, wherein the gate of the select transistor is formed substantially vertically and perpendicular to the gate of the first transistor relative to a vertical plane.

20. (Amended) A memory device having a square feature size of less than $4F^2$ comprising:

a substrate having at least one semiconductor layer;

a first n-type layer formed over the substrate;

a p-type layer formed over the first n-type layer;

a second n-type layer formed over the p-type layer;

a floating gate formed over the substrate;

a trench formed in the ~~substrate~~p-type layer; and

a select gate formed on a sidewall of the trench.

21. (Amended) A memory device having a square feature size of less than $4F^2$ comprising:

a substrate having at least one semiconductor layer;

a first n-type layer formed over the substrate forming a source;

a p-type layer formed over the first n-type layer forming a vertical channel;

a second n-type layer formed over the p-type layer forming a drain;

a tunnel oxide layer formed over at least a portion of the second n-type layer;

a first poly layer formed over at least a portion of the tunnel oxide layer;

trenches formed in the ~~substrate~~p-type layer; and

a select gate form d on sidewalls of the trenches.

22. (Amended) A memory device having a square feature size of less than $4F^2$ comprising:

a substrate having at least one semiconductor layer, said substrate comprising:;

a buried source formed ~~over~~in the substrate;

a vertical channel formed over the buried source; and

a drain formed over the vertical channel;

a tunnel oxide layer formed over at least a portion of the drain;

a ~~self-aligned~~ floating gate formed over the tunnel oxide layer; such that at least a portion of the floating gate overlies at least a portion of the drain;

a select trench formed in the substrate;

a select gate formed along sidewalls of the select trench;

an active trench formed generally over~~in~~ the ~~substrate~~drain; and

a conductive layer formed in the active trench; ~~and~~

~~a select gate formed along sidewalls of the active trench area.~~.

23. (Twice Amended) A memory device having a square feature size of less than $4F^2$ comprising:

a first n-type layer formed over a substrate;

a p-type layer formed over the n-type layer;

a second n-type layer formed in the p-type layer;

a select trench formed in the ~~substrate~~p-type layer;

a vertical select gate formed in the select trench;

digitlines ~~are~~ formed over, and capable of electrical communication with the second n-type layer;

a ~~self-aligned~~ floating gate formed over the ~~n~~p-type layer such that at least a portion of the floating gate overlies at least a portion of the second n-type layer; and

wordlines formed over the substrate and the digitlines.

26. (Twice Amended) A memory device comprising:

a first n-type layer formed over a substrate ~~forming~~ defining a source;

a p-type layer formed over the n-type layer;

a s cond n-type layer formed in the p-type layer ~~forming~~ defining a drain;

a select trench formed in the ~~substrate~~p-type layer;

a select gate formed substantially vertical in the select trench~~, wherein the memory device has a feature size substantially less than $4.5F^2$~~.; and

a floating gate formed over the p-type layer so as to avoid the select trench.